



DEDAN KIMATHI UNIVERSITY
TECHNOLOGY

OF

University Examinations 2021/ 2022
FIRST YEAR FIRST SEMESTER EXAMINATION FOR THE IBSC. I.T

EEE 2206 DIGITAL LOGIC

SUPPLEMENTARY/SPECIAL

Date

Time

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Instructions

1. Answer question one and any other two questions
2. Use standard notation and SI units only
3. No casual freehand drawings allowed

QUESTION ONE (COMPULSORY) 30 Marks

- (a) Classify the following systems into analogue or digital systems:
- (i) Time on the Clock at Parliament Buildings in Nairobi
 - (ii) Metre ruler
 - (iii) Green and red traffic lights
 - (iv) Voice from an loudspeaker
 - (v) An electric toggle switch
 - (vi) Number of bananas in a basket
 - (vii) Keys on a piano keyboard
 - (viii) TV image **(4 marks)**
- (b) Implement a two-input XNOR gates using NAND gates only **(3 marks)**
- (c) Define briefly a “tristate logic gate”. What is the main use of “tristate logic gate”. Give the logic diagram of a tristate buffer gate **(3 marks)**
- (d) Give a logic diagram (gate level) of a binary to decimal decoder **(4 marks)**

- (e) Minimize the following 4-variable digital function using a K-map: $f(x) = \sum m(0, 1, 4, 5, 6, 7, 8, 9, 12, 13)$ and implement with NAND gates it **(4 marks)**
- (f) What is the unique feature of TTL logic family? Explain **(4 marks)**
- (g) Give the circuit (gate-level) of a basic D- flip-flop and its waveforms **(4 marks)**
- (h) What is called a “universal shift register”. Give an IC number and pin configuration of such a register **(4 marks)**

QUESTION TWO (Optional)

- (a) Compare with some comment TTL and CMOS logic family In terms (i) level of integration (ii) power consumption (iii) speed **(3 marks)**
- (b) Give and comment a basic circuit diagram(transistor level) of a CMOS NAND gate **(3 marks)**
- (c) For the transistor in Fig.1., find the range of V_{BB} for the transistor to be
- In the cut-off region
 - In the active region
 - In the saturation region **(6 marks)**

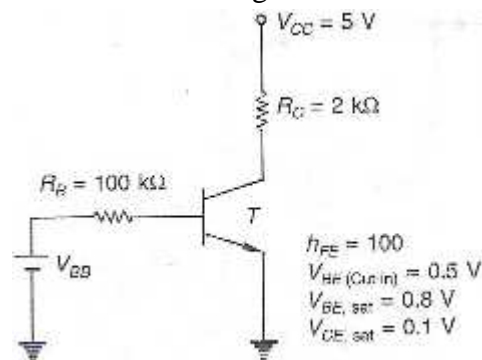


Fig.1. For Question Two (c)

- (d) What the main advantage and main disadvantage of ECL logic family **(2 marks)**
- (e) What is meant by 74ALSXX logic family? Comment on this logic family **(4 marks)**
- (f) Define the specification” Noise margin” for a given logic family **(2 marks)**

QUESTION THREE (Optional)

- (a) (i) What determine the colour of an LED? **(2 mark)**
(ii) Give the mathematical expression **(2 marks)**
- (b) Compare LEDs and LCD seven-segment displays. Give two popular IC used in each type of display **(4 marks)**
- (c) Give the logic diagram(gate level) of a decimal to binary encoder **(4 marks)**

- (d) State and explain three applications of multiplexers (3 marks)
- (e) Implement the logic function $Y(A,B,C,D)=AB+BD+BCD$ using a 8:1 MUX (3 marks)
- (f) Name a popular IC number of a full adder (2 marks)

QUESTION FOUR (optional)

- (a) Given the function in SOP form: $f(A,B,C,D)= m(5, 7, 12, 13, 14, 15)$
 - (i) Give its truth table (2 marks)
 - (ii) Give its Karnaugh map (2 marks)
 - (iii) Minimize it using Karnaugh map and implement it using 2-input NAND gates (3 marks)
- (b) (i) Minimize using Karnaugh maps: $f(PQRS) = m(0,3,4,7,8) + d(10,11,12,13,14,15)$ (5 marks)
 - (ii) Implement the same with NAND gates (4 marks)
 - (iii) If at Nerokas Engineering Solutions, one 74LS00 costs 50 KES, how much will implementation cost? (4 marks)

QUESTION FIVE (optional)

- (a) (i) Give the logic diagram of an S-R flip-flop with a PRESET and CLEAR inputs (3 marks)
 - (ii) With the aid of logic symbol transform it into a J-K flip-flop I one hand (3 marks)
 - (iv) Then transform it into a D-flip-flop in the other hand (2 marks)
- (b) (i) What is modulus of a counter (1 mark)
 - (ii) Give the circuit of a decade counter (3 marks)
- (c) Explain the main difference between a register and a counter (2 marks)
- (d) State and explain 3 uses of counters (3 marks)
- (e) Give the logic diagram of a 4-bit SISO register using D-flip-flops (3 marks)

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